CentraleSupélec | université PARIS-SACLAY

CENTRALESUPELEC RECRUTE

Assistant Professor in Embedded Electronics for Intelligent Connected Systems

CDI de droit public

Contexte

CentraleSupélec is a public scientific, cultural, and professional institution (EPSCP in French) under the authority of the French ministers for higher education and industry. Its primary missions are training high-level scientific general engineers, engineering and systems sciences research, and executive education. As part of its development, CentraleSupélec is looking for an assistant professor to join the Rennes campus of CentraleSupélec and carry out research in the IETR (Institute of Electronics and Digital Technologies, UMR CNRS 6164) laboratory.

The Rennes campus of CentraleSupélec operates courses in the general CentraleSupélec course, both in the FISA (Training of Engineers under Apprentice Status) and FISE (Training of Engineers under Student Status) pathway, over the three years of the engineering cycle. The Rennes campus thus offers three-year concentrations of the general engineer curriculum, including the one entitled NUVI (Numérique et Vivant) in line with the desired position profile.

There are six departments in the IETR laboratory, with the Signal and Communications (SC) department being among them. SIGNAL and ASIC are the two research teams in the SC department. The hired person is expected to conduct research in the ASIC (Architecture, Systems, Infrastructure and Electronics) team. The ASIC team's research work covers the entire spectrum, from the adequacy algorithm architecture of intelligent connected systems to hardware proof of concept (hardware realisation), with considerations for throughput, power consumption, reliability, and safety.

Education task

The workload associated with the position corresponds to statutory teaching service, i.e. 192 hours of TD equivalent per year. Teaching activities will be carried out over a broad spectrum covering the lessons taught

- to students of CentraleSupélec's two specialised engineering programs, "Electronics" and "Digital Systems".
- To students of CentraleSupélec's general engineering curriculum in particular:
  - In the first year of the apprenticeship sector (FISA)
  - In the third year as part of the "Numérique et Vivant" concentration.

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These activities will take the following forms:

- In initial training: active participation in supervising laboratory work and projects and monitoring of students (internships, gap year, professionalisation contract, etc.)
- In continuing education: tutorials or specialised courses on specific subjects related to the candidate's area of expertise

The subjects taught include skills in low/high-frequency analogue electronics, digital electronics, hardware accelerators for AI, embedded architectures, the design of systems on chips, and, more generally, a knowledge of the challenges of the digital transition and technological sovereignty. The candidate must be able to teach in English.
The candidate must demonstrate interdisciplinary openness and contribute to various teaching teams. The candidate will have to be a driving force for the improvement and evolution of programs regarding digital transition issues faced by companies and citizens, under the responsibility of the training department and the various program managers.

Research mission

The research activities will be carried out within the ASIC research team (https://www.ietr.fr/equipe-asic-architecture-systems-infrastructure-and-electronics) component of the IETR (Institute of Electronics and Digital Technologies) Mixed unit of Research from CentraleSupélec, the CNRS, the University of Rennes, the University of Nantes and the INSA of Rennes.

The objective of the research activities associated with the position will be to strengthen the design of high-performance, low-power, reliable, and secure intelligent embedded systems. Embedded heterogeneous architectures, hardware optimisation techniques, algorithmic optimisation techniques, and integration of artificial intelligence mechanisms will be the main themes to develop. The person recruited must have the expertise to contribute to designing and implementing intelligent, embedded and high-performance systems, with the ambition to offer reliable, secure, innovative, sustainable, and energy-efficient solutions. The application areas are mainly 5G/6G wireless communication systems and digital health.

Candidate profile

The candidate must hold a Ph.D. degree in electronics with research work related to embedded artificial intelligence (design and implementation). The candidate must be the author or co-author of publications in international journals (publication requirement will depend on the curriculum vitae and the number of years of experience). Furthermore, the person recruited must have a taste for teaching, research (academic and contractual in relation to industry), and teamwork. Finally, the candidate must engage in the supervision of research work related to the themes of the ASIC team.

Selection procedure

Candidates must send before November, 25th 2024, by email only, to the following email address, drh.pole-enseignant@centralesupelec.fr with reference MCF-IETR-ASIC-Electronique Embarquée-Rennes-2412 a file in PDF format including:

· A cover letter
· A detailed CV (teaching experience, research, mobility, publications, etc.)
· A research and teaching project adapted to CentraleSupélec (5 to 10 pages)
· A copy of the identity card or passport
· A copy of the doctoral degree and any document attesting to research supervision experience
. Thesis defense report
· Letters of recommendation (optional)

· And any documents that attest to previous experience

Recruitment interview

For the candidates selected for the audition, the audition will take place in three stages:

- A presentation of the candidate's background and teaching and research project;
- An illustration of a lesson in English on a problem whose subject is identical for all candidates will be specified on the invitation.
- An exchange with the members of the committee.

The duration of the three presentations will be specified in the audition invitations.

Scientific contacts

- Amor Nafkha, member of the IETR ASIC team and co-head of the the specialisation course "Electronics"
  - Amor.nafkha@centralesupelec.fr

- Yves Louet, director of the Rennes campus of CentraleSupelec: yves.louet@centralesupelec.fr